Claims:

1. A semiconductor memory including a memory cell array constituted of a number of memory cells arranged in the form of a matrix having a number of rows and a number of columns, and a defective memory cell relief means, wherein said memory cell array includes main memory cells arranged in the form of a matrix having a number of rows and a number of columns, at least one row of substitution information storing memory cells and at least one column of redundant memory cells, and said defective memory cell relief means includes a means for operating, in place of a column including a defective memory cell, a non-defective column adjacent to said column including the defective memory cell.

2. A semiconductor memory claimed in Claim 1 wherein said defective memory cell relief means includes a means for inhibiting access to said column including the defective memory cell in accordance with the content of said substitution information storing memory cells, a means for operating, in place of the column including a defective memory cell within said main memory cells, a non-defective column within said main memory cells, adjacent to said column including the defective memory cell, and a means for compensating shortage in said main memory cells with said redundant memory cells.

3. A semiconductor memory claimed in Claim 2 wherein said defective memory cell relief means includes a control circuit for generating a control signal on the basis of the content of said substitution information storing memory cells.

4. A semiconductor memory claimed in Claim 3 wherein said defective memory cell relief means further includes a Y selection circuit receiving a Y selection signal and said control signal for selecting one column of the columns in said memory cell array to connect a bit line of the selected column to an input/output line.

5. A semiconductor memory claimed in Claim 4 wherein said control circuit generates first and second control signals, and said Y selection circuit receives a first Y selection signal and said first and second control signals to connect said bit line of the selected column to either a first input/output line or a second input/output line.

6. A semiconductor memory claimed in Claim 4 wherein said control circuit generates first and second control signals, and said Y selection circuit receives first and second Y selection signals and said first and second control signals to connect said bit line of the selected column to said input/output line.

7. A semiconductor memory claimed in Claim 3 wherein said control circuit includes at least "n" bits of volatile memory cells for storing the substitution information of "n" bits stored in one row of substitution information storing memory cells.

8. A semiconductor memory claimed in Claim 7 wherein said control circuit further includes a decoder receiving the substitution information

stored in said at least "n" bits of volatile memory cells, for generating said control signal.

9. A semiconductor memory claimed in Claim 3 wherein only said substitution information storing memory cells are a non-volatile memory cell.

10. A semiconductor memory claimed in Claim 3 wherein said main memory cells, said redundant memory cells and said substitution information storing memory cells are a non-volatile memory cell.

11. A semiconductor memory claimed in Claim 10 wherein said non-volatile memory cell is a ferroelectric non-volatile memory cell.

12. A semiconductor memory including first and second memory cell arrays each constituted of a number of memory cells arranged in the form of a matrix having a number of rows and a number of columns, and a defective memory cell relief means, wherein each of said first and second memory cell arrays includes main memory cells arranged in the form of a matrix having a number of rows and a number of columns, at least one row of substitution information storing memory cells and at least one column of redundant memory cells, the substitution information for said first memory cell array being stored in said substitution information storing memory cells in said second memory cell array, the substitution information for said second memory cell array being stored in said substitution information storing memory cells in said first memory cell array, so that when said first memory cell array is accessed,

substitution information is simultaneously read out from said substitution information storing memory cells in said second memory cell array in order to relieve a defective memory cell within said first memory cell array.

13. A semiconductor memory claimed in Claim 12 wherein only said substitution information storing memory cells are a non-volatile memory cell.

14. A semiconductor memory claimed in Claim 12 wherein said main memory cells, said redundant memory cells and said substitution information storing memory cells are a non-volatile memory cell.

15. A semiconductor memory claimed in Claim 14 wherein said non-volatile memory cell is a ferroelectric non-volatile memory cell.

16. A semiconductor memory including a memory cell array constituted of a number of memory cells arranged in the form of a matrix having a number of rows and a number of columns, and a defective memory cell relief means, wherein said memory cell array includes main memory cells arranged in the form of a matrix having a number of rows and a number of columns and at least one column of redundant memory cells, and said defective memory cell relief means includes at least "n" bits of ferroelectric non-volatile memory cells, for storing substitution information of "n" bits.

17. A semiconductor memory claimed in Claim 16 wherein each of said at least "n" bits of ferroelectric non-volatile memory cells comprises two ferroelectric capacitors and at least four transistors.

18. A semiconductor memory comprising

a memory cell array including main memory cells arranged in the form of a matrix having a number of rows and a number of columns, at least one row of substitution information storing memory cells and at least one column of redundant memory cells, said substitution information storing memory cells being constituted of a rewritable non-volatile memory cell;

a Y selection circuit associated with said memory cell array and receiving a Y selection signal to connect an input/output line to a bit line of the column designated by said Y selection signal;

a control circuit for generating a control signal, when substitution information read out from said substitution information storing memory cells before an ordinary reading/writing operation indicates that a column including a defective memory cell should be replaced with another column having no defective memory cell, said control signal being supplied to said Y selection circuit for inhibiting access to said column including the defective memory cell and for replacing said column including the defective memory cell by one column of the other columns and said at least one column of redundant memory cells,

said Y selection circuit being so configured that when the column designated by said Y selection signal is said column including the defective memory cell, said Y selection circuit selects a column adjacent to the column designated by said Y selection signal, and connects said

input/output line to a bit line of the selected column adjacent to the column designated by said Y selection signal.

19. A semiconductor memory claimed in Claim 18 wherein said Y selection circuit is controlled by said control signal to select the column designated by said Y selection signal, until a column just before said column including the defective memory cell, and to select, a column adjacent to the column designated by the Y selection signal for the column designated by the Y selection signal and succeeding columns.

20. A semiconductor memory claimed in Claim 18 wherein said memory cell array includes (0)th to (j)th columns of main memory cells and a (j+1)th column of redundant memory cells, and said Y selection circuit includes:

a first series circuit composed of a first Y switch and a first control switch connected in series between said input/output line and a bit line of a (k)th column (k=1 to (j+1)) excluding the (0)th column, said first Y switch being on-off controlled by a Y selection signal corresponding to a (k-1)th column, and said first control switch being on-off controlled by a control signal CS(k-1) generated from the data read out from the substitution information storing memory cell corresponding to said (k-1)th column, and

a second series circuit composed of a second Y switch and a second control switch connected in series between said input/output line and a bit line of a (k-1)th column excluding the (j+1)th column, said second Y switch being on-off controlled by said Y selection signal corresponding to said (k-1)th column, and said second control switch being on-off

controlled by an inverted signal of said control signal CS(k-1) generated from the data read out from the substitution information storing memory cell corresponding to said (k-1)th column.

21. A semiconductor memory claimed in Claim 18 wherein said substitution information storing memory cells are read and written by use of a writing/reading circuit for said main memory cells.

22. A semiconductor memory claimed in Claim 18 wherein each of said substitution information storing memory cells includes a ferroelectric capacitor having one end connected to a plate line and a cell transistor connected between a bit line and the other end of said ferroelectric capacitor, said cell transistor having a gate connected to a word line.

23. A semiconductor memory claimed in Claim 18 wherein each of said main memory cells includes a ferroelectric capacitor having one end connected to a plate line and a cell transistor connected between a bit line and the other end of said ferroelectric capacitor, said cell transistor having a gate connected to a word line.

24. A semiconductor memory claimed in Claim 18 wherein said control circuit includes a memory circuit for receiving and holding the substitution information read out from said one row of substitution information storing memory cells, and said control circuit generates said control signal on the basis of the substitution information held in said memory circuit.

25. A semiconductor memory claimed in Claim 18 wherein, in response to one Y selection signal, a plurality of bit lines are simultaneously selected and connected to a plurality of input/output lines, and when the selected plurality of bit lines includes a bit line connected to the column including the defective memory cell, the a bit line connected to the column including the defective memory cell is not selected, and a bit line of a column adjacent to the column including the defective memory cell is selected.

26. A semiconductor memory claimed in Claim 18 wherein the substitution information includes a plurality of bits indicative of an address of one column within said memory cell array excluding said column of redundant memory cells, and an information bit indicative of substitution or non-substitution, and

wherein word lines of said memory cell array excluding said row of substitution information storing memory cells are divided into a plurality of groups of word lines, and one substitution information is allocated to each one group of word lines, so that a substitution column can be different from one group of word lines to another group of word lines, whereby even if a plurality of defective memory cells exist in different columns, the defective memory cells can be relieved.

27. A semiconductor memory claimed in Claim 26 wherein said control circuit selects substitution information for a group of word lines to be accessed, from the substitution information read out from said one row of substitution information storing memory cells excluding said column of

redundant memory cells, and said control circuit generates said control signal on the basis of the selected substitution information.

28. A semiconductor memory claimed in Claim 26 wherein substitution information for a group of word lines to be accessed is selected on the basis of a signal obtained by decoding a bit or bits identifying said plurality of groups of word lines, of an X address, and the selected substitution information is supplied to a decode circuit, which generates said control signal to said Y selection circuit.

29. A semiconductor memory claimed in Claim 28 wherein said control circuit includes memory cells of the number corresponding to the number of columns in said memory cell array excluding said column of redundant memory cells, each of said memory cells storing the data read out from a corresponding memory cell of said row of substitution information storing memory cells, and

wherein said substitution information for a group of word lines to be accessed is selected from the substitution information stored in said memory cells of said control circuit, on the basis of a signal obtained by decoding a bit or bits identifying said plurality of groups of word lines, of an X address, and the selected substitution information is supplied to said decode circuit.

30. A semiconductor memory claimed in Claim 18 wherein when a power supply is turned on, data is read out from said substitution information storing memory cells.

31. A semiconductor memory comprising a memory cell array divided into a plurality of sub-arrays coupled through a local bus, each of said sub-arrays including a number of main memory cells arranged in the form of a matrix having a number of rows and a number of columns, at least one row of substitution information storing memory cells and at least one column of redundant memory cells, each of said sub-arrays being associated with a Y selection circuit and a plurality of sense amplifiers each provided for a bit line of one corresponding column,

wherein in the bit line of each column, a transfer gate is inserted between said substitution information storing memory cells and said main memory cells and said redundant memory cells, and is controlled by a separation control signal to separate said main memory cells and said redundant memory cells from the associated sense amplifiers and said substitution information storing memory cells,

wherein a pair of said sub-arrays are mated so that said substitution information storing memory cells in each of said pair of sub-arrays store substitution information for the other of said pair of sub-arrays, and when one of said pair of sub-arrays is read out, the substitution information for said one of said pair of sub-arrays is read out from said substitution information storing memory cells in the other of said pair of sub-arrays while separating said main memory cells and said redundant memory cells in the other of said pair of sub-arrays from the associated sense amplifiers and said substitution information storing memory cells in the other of said pair of sub-arrays by turning off said transfer gates in the other of said pair of sub-arrays, and the read-out substitution information is transferred through said local bus, as a control signal, to said Y selection circuit associated with said one of said pair of sub-arrays,

so that said Y selection circuit associated with said one of said pair of sub-arrays receives a Y selection signal and said control signal, to connect the bit line of the column designated by said Y selection signal to an input/output line when said control signal indicates that the column designated by said Y selection signal is not a column including a defective memory cell, and to connect said input/output line to a column adjacent to the column designated by said Y selection signal when said control signal indicates that the column designated by said Y selection signal is a column including a defective memory cell.

32. A semiconductor memory claimed in Claim 31, wherein word lines of each sub-array excluding said row of substitution information storing memory cells are divided into a plurality of groups of word lines, and one substitution information is allocated to each one group of word lines, so that a substitution column can be different from one group of word lines to another group of word lines, whereby even if a plurality of defective memory cells exist in different columns, the defective memory cells can be relieved, and

further including a selection circuit for selecting substitution information for a group of word lines to be accessed, on the basis of a signal obtained by decoding a bit or bits identifying said plurality of groups of word lines, of an X address, and a decode circuit receiving the selected substitution information for generating said control signal which is supplied through said local bus to said Y selection circuit of the other sub-array.

33. A semiconductor memory comprising:

a memory cell array including a number of main memory cells arranged in the form of a matrix having a number of rows and a number of columns and at least one column of redundant memory cells;

a plurality of sense amplifiers each provided for a bit line of one corresponding column in said memory cell array;

a Y selection circuit associated with said memory cell array;

a control circuit including a plurality of substitution information storing memory cells for generating, on the basis of substitution information read out from said substitution information storing memory cells, a control signal to said Y selection circuit for inhibiting access to a column including a defective memory cell and for replacing said column including the defective memory cell by one column of the other columns and said at least one column of redundant memory cells,

wherein when a power supply is turned on, said substitution information is read out from said substitution information storing memory cells, and said Y selection circuit receiving a Y selection signal and said control signal, connects the bit line of the column designated by said Y selection signal to an input/output line when said control signal indicates that the column designated by said Y selection signal is not a column including a defective memory cell, and to connect said input/output line to a column including no defective memory cell when said control signal indicates that the column designated by said Y selection signal is a column including a defective memory cell.

34. A semiconductor memory claimed in Claim 33, wherein said substitution information storing memory cells of said control circuit is

formed of a ferroelectric memory cell having a ferroelectric capacitor formed above a memory transistor.

35. A semiconductor memory claimed in Claim 33, wherein word lines of said memory cell array excluding said row of substitution information storing memory cells are divided into a plurality of groups of word lines, and one substitution information is allocated to each one group of word lines, so that a substitution column can be different from one group of word lines to another group of word lines, whereby even if a plurality of defective memory cells exist in different columns, the defective memory cells can be relieved, and

wherein substitution information for a group of word lines to be accessed is selected on the basis of a signal obtained by decoding a bit or bits identifying said plurality of groups of word lines, of an X address, and the selected substitution information is supplied to a decode circuit, which generates said control signal to said Y selection circuit.

36. A semiconductor memory claimed in Claim 35 wherein said control circuit includes memory cells of the number corresponding to the number of columns in said memory cell array excluding said column of redundant memory cells, each of said memory cells storing the data read out from a corresponding memory cell of said substitution information storing memory cells, and

wherein said substitution information for a group of word lines to be accessed is selected from the substitution information stored in said memory cells of said control circuit, on the basis of a signal obtained by decoding a bit or bits identifying said plurality of groups of word lines,

of an X address, and the selected substitution information is supplied to said decode circuit.